A Planar Broadband Balanced Doubler Using a Novel Balun Design

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Abstract— **We report on the design and measurement of a broadband MIC balanced varactor frequency doubler. The design incorporates a novel balun to achieve a grounded CPW-to-slotline transition. The balanced structure offers inherent isolation in the output port from all odd harmonics including the fundamental frequency. Measurements show a port-to-port conversion loss between 8 and 10 dB over an output frequency range of 6–10 GHz. The design can be easily scaled to millimeter-wave frequencies using a monolithic approach.**

I. Introduction

MONOLITHIC broadband balanced doublers have been demonstrated in the literature using varistor diodes [1], [2]. However, the varistor diodes are theoretically limited in their possible conversion efficiencies [3], and the theoretical conversion loss of an ideal full-wave varistor rectifier is 7.4 dB [1]. The current varactor designs are either narrowband [4] or have not yet demonstrated a high conversion efficiency [5]. In this letter, we present a balanced varactor multiplier that is based on grounded-CPW and slotline transmission media together with Schottky varactor diodes. A novel balun is designed to achieve the necessary grounded CPW-to-slotline transition, and a wideband 6–10 GHz output frequency doubler is achieved.

II. Doubler Design

An efficient design for a broadband multiplier utilizes varactor diodes in a full-wave rectifier configuration [4], [5]. In this case, it is necessary to apply a negative DC bias to the diodes. The isolation at the output port of the odd harmonics will still be present, and the conversion loss will be limited in theory by impedance-matching considerations (Manley and Rowe relations [6]).

A varactor doubler in a full-wave rectifier configuration is shown in Fig. 1, along with its associated equivalent circuit. The design utilizes grounded CPW and slotline transmission lines on a high-dielectric-constant substrate (ϵ_r=10.2) to approximately simulate a millimeter-wave GaAs integrated circuit. To prevent radiation from the grounded CPW line into substrate modes, it is necessary to place via holes at a distance

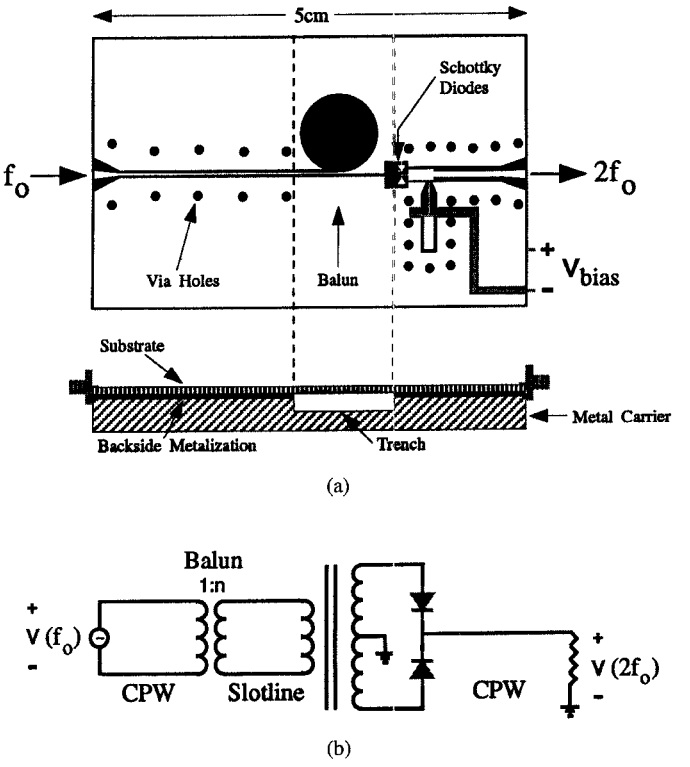

Fig. 1. Doubler layout with a trench in the metal carrier under the balun (a) and equivalent circuit used in CAD simulations (b).

less than or equal to λ_{eff} [4], [5], where λ_{eff} is the effective wavelength of the odd transmission line mode.

A novel broadband balun is designed to achieve the grounded CPW-to-slotline transition (Fig. 2). The balun is based on a broadband CPW-to-slotline transition [7]. By not metalizing the backside underneath the slotline and circular patch and including a trench in the fixture under the absent metalization, a wideband balun is achieved. The circular patch radius is chosen to appear as an approximate open circuit over the desired frequency range [8]. A back-to-back balun with a center frequency of 5 GHz was fabricated on ϵ_r=10.2, 1.27-mm-thick Duroid. The grounded CPW and slotline impedance are 50Ω. Fig. 2(b) shows the measured port-to-port return and insertion loss with a 2.5-mm trench and a 7.5-mm-diameter circular patch. The port-to-port measurements include 0.3 dB of ohmic and radiative loss in the grounded CPW lines. It is seen that the loss per transition is less than 0.4 dB at 5 GHz over a ±10% bandwidth. The optimum trench depth was

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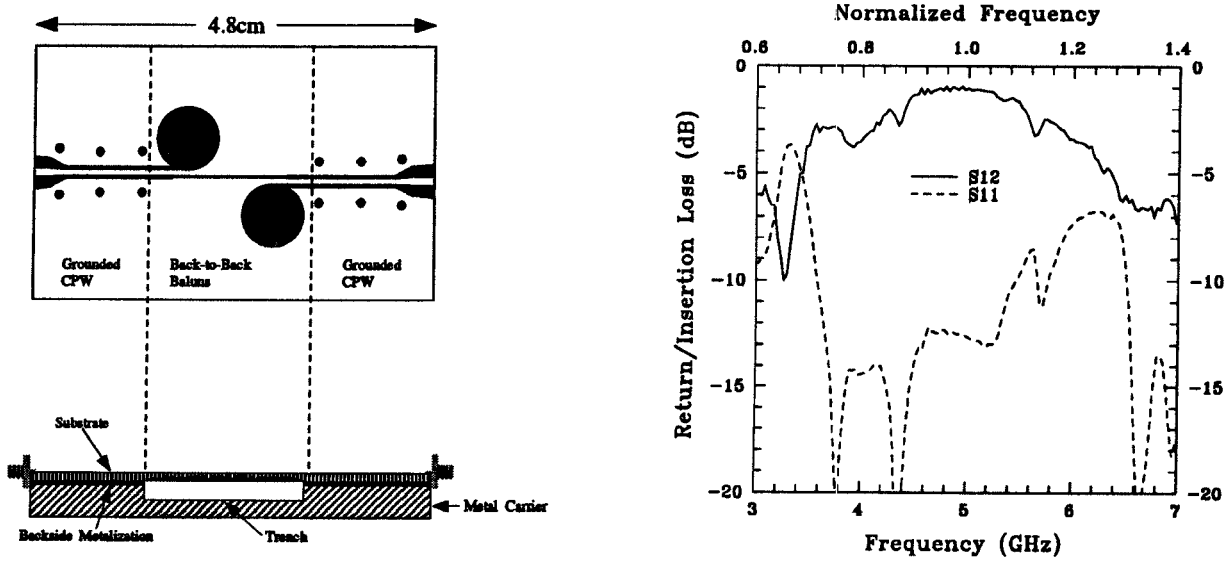


(a) (b)

Fig. 2. Back-to-back grounded CPW-to-slotline balun with a trench in the metal carrier under the baluns (a) and measured port-to-port return/insertion losses (b).

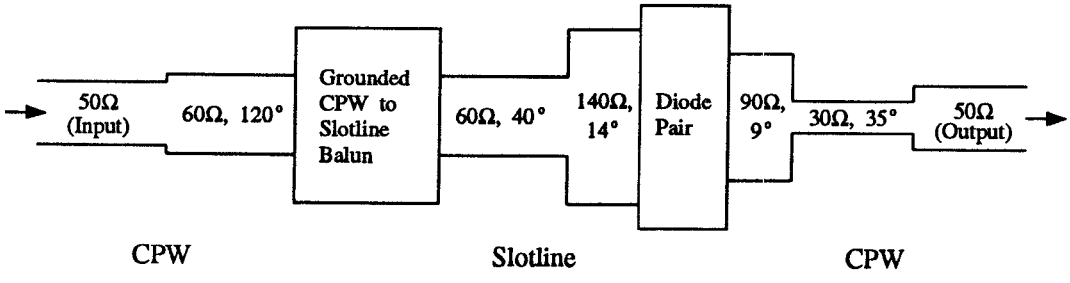


Fig. 3. The CPW and slotline-matching network used in the balanced doubler circuit.

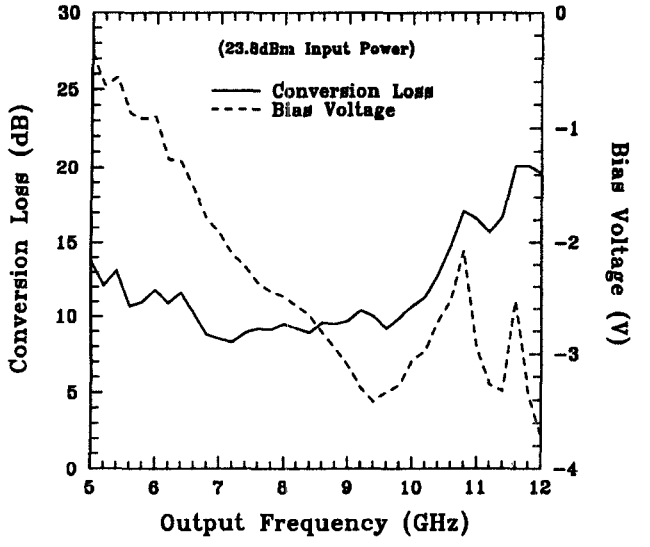
empirically determined by increasing the depth until there was no more observable change in the S-parameters.

Fig. 3 shows the wideband impedance-matching network. A 60-Ω grounded CPW and slotline impedance were used in the input to simplify fabrication (50-Ω slotline would be extremely narrow) [9]. The short, 140-Ω section of slotline appears inductive (j35 Ω) to resonate out the capacitance of the diodes (-j40 Ω). A 30-Ω impedance section was added at the output to optimize matching of the the second harmonic, since the output impedance of the balanced varactor multiplier is low (about 20Ω). Although a more complex impedance network might yield a higher conversion efficiency, the network was intentionally made as simple as possible to maximize the bandwidth and to simplify the fabrication. The theoretical conversion efficiencies are calculated using EEsof Libra software [10] and the impedance network of Fig. 3 using the varactor diode ALPHA CVH-2030-01, which has parameters of C_{j0}=0.5 pF, R_s=2 Ω, and γ=0.5. The analysis assumes a lossless balun with a 1:1 turns ratio and neglects the loss in the input and output transmission lines and in the bias network. The analysis indicates that a high conversion efficiency of 5.5–7.5 dB can be achieved over a broad bandwidth (6–11 GHz).

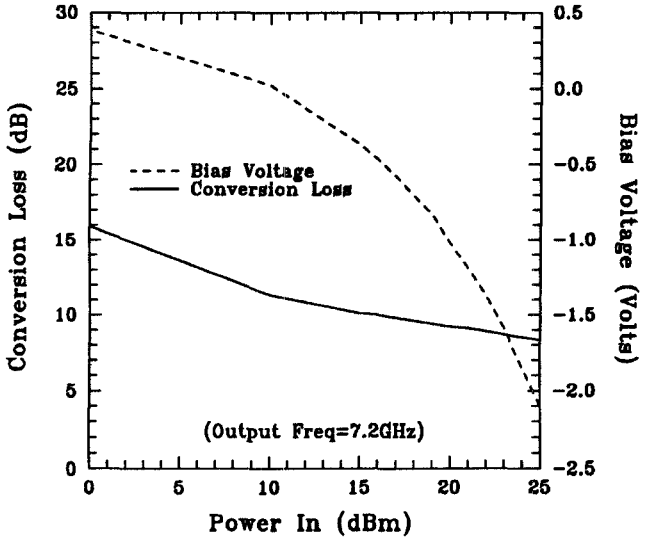
III. Measurements

A balanced varactor doubler was fabricated on an ϵ_r=10.2, 1.27-mm-thick Duroid substrate for an input center frequency of 4 GHz. The varactors were hybridly mounted at the CPW/slotline junction. Via holes were placed every 5 mm on the input side, corresponding to a maximum input frequency of 6 GHz, and 2.5 mm on the output side, corresponding to a maximum output frequency of 12 GHz. The input and output ports were connected to standard SMA connectors.

Fig. 4 shows the measured port-to-port conversion loss as a function of the output frequency at a constant input power of 23.8 dBm. The bias voltage has been adjusted at



(a)



(b)

Fig. 4. Measured port-to-port conversion loss versus frequency (a) and versus input power (b). In (a), a bias of -2.5 V yields approximately the same conversion curve.

each frequency for best performance, although a constant bias of -2.5 V yields approximately the same conversion curve. The bias voltage becomes more negative with frequency to present a constant diode reactance to the circuit (except at the highest frequencies where the balun, bias section, etc. begin creating impedance mismatches). The corresponding DC current is 20–60 μA (depending on frequency), indicating a predominantly varactive mode of operation. The loss in the transmission lines and baluns are estimated to be 1.8 dB (see Fig. 1 for doubler layout). The measured port-to-port conversion loss is less than 10 dB for an output frequency between 6.4–10 GHz. The best performance is 8.3-dB port-to-port conversion loss at 7.2 GHz, and is equivalent to a diode conversion efficiency of 6.5 dB. The measured data agrees well with the theoretical predictions of 5.5–7.5 dB conversion efficiency.

The best isolation was achieved at the output center frequency of 8 GHz and resulted in first and third harmonics at the output port that are -25 dB below the second harmonic. The isolation is -20 dB at ± 1 GHz and -15 dB at ± 2 GHz away from the center frequency. This is due to the bias section, which is designed for a center output frequency of 8GHz.

A millimeter-wave monolithic doubler with an output frequency of 60–90 GHz is currently being built using a scaled design at the University of Michigan and NRAO.

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